**WHAT IS CLAIMED IS:**

1. A clock recovery circuit in which a timing jitter in a recovered clock is suppressed, the clock recovery circuit comprising:

transceiver means for supplying a data signal, which is based on serial data having a regular bit pattern during a first period, and is based on serial data having an arbitrary bit pattern during a second period following the first period;

a duty factor controller for adjusting a data transition characteristic of the transceiver means so as to reduce a duty factor error in a data signal supplied from the transceiver means in the first period, and having the adjusted data transition characteristic stored; and

a clock recovery unit for recovering, from the data signal supplied from the transceiver means, a clock synchronized with the data signal in the second period.

2. The clock recovery circuit of claim 1, wherein the transceiver means includes:

a driver for supplying a differential data signal; and

a receiver for receiving the differential data signal from the driver and supplying a single end signal corresponding to the differential data signal,

wherein a data transition characteristic of the driver or the receiver is adjusted by the duty factor

controller.

3. The clock recovery circuit of claim 1, wherein the duty factor controller includes an integrator circuit for integrating the data signal so as to output an analog voltage representing a duty factor error in the data signal.

4. The clock recovery circuit of claim 3, wherein the duty factor controller further includes an analog-to-digital converter for giving the transceiver means a digital signal according to the analog output voltage from the integrator circuit as a duty factor control signal.

5. The clock recovery circuit of claim 1, wherein the duty factor controller includes:

a delay circuit for generating a delayed data signal that is delayed by one data interval with respect to the data signal; and

a logic circuit for giving the transceiver means a duty factor control signal according to a plurality of logical operation results of the data signal and the delayed data signal.

6. The clock recovery circuit of claim 1, wherein the duty factor controller includes means for detecting a phase error in the clock with respect to the data signal and giving the transceiver means a duty factor control signal according to a magnitude of the phase error.

7. A clock recovery unit for recovering a clock synchronized with a given data signal, the clock recovery

unit comprising:

a voltage controlled oscillator for generating a clock having a frequency according to a control voltage;

a first charge pump and a second charge pump whose respective outputs are coupled to a common node;

a first phase detector for detecting a phase error in the clock with respect to one of a rising edge and a falling edge of the data signal so as to control the first charge pump according to the phase error; and

a second phase detector for detecting a phase error in the clock with respect to the other edge of the data signal so as to control the second charge pump according to the phase error,

wherein a voltage that is generated at the common node by the first and second charge pumps is given to the voltage controlled oscillator as the control voltage so that the phase error detected by the first phase detector and the phase error detected by the second phase detector are both reduced.

8. The clock recovery unit of claim 7, wherein the data signal is a data signal of an NRZ format.

9. The clock recovery unit of claim 7, further comprising means for controlling a transition characteristic of the data signal according to an output of one of the first and second phase detectors.

10. The clock recovery unit of claim 7, further

comprising:

a first delay circuit inserted in a data input path of the second phase detector;

a second delay circuit inserted in a clock input path of the second phase detector; and

a third phase detector for detecting a phase error in an output of the second delay circuit with respect to an output of the first delay circuit and adjusting a delay amount of the first or second delay circuit so as to reduce the phase error.

11. The clock recovery unit of claim 10, wherein:

there is provided a period in which the first delay circuit receives, instead of the data signal, an adjustment signal based on serial data having a regular bit pattern; and

when the third phase detector detects a lag phase error in an output of the second delay circuit with respect to an output of the first delay circuit in response to the adjustment signal, the third phase detector increases a delay amount of the first delay circuit so as to reduce the lag phase error, and has the increased delay amount stored, whereas when the third phase detector detects a lead phase error in the output of the second delay circuit with respect to the output of the first delay circuit in response to the adjustment signal, the third phase detector increases a delay amount of the second delay circuit so as to reduce the lead phase error, and has the increased delayed amount stored.

12. The clock recovery unit of claim 10, further comprising:

a third delay circuit for outputting the data signal while delaying the data signal by one half of the delay amount of the first delay circuit; and

a fourth delay circuit for outputting the clock while delaying the clock by one half of the delay amount of the second delay circuit.